Review of SiGe Process Technology and its Impact on RFIC Design

Amitava Das, Margaret Huang, Jyoti Mondal, Daniel Kaczman, Carl Shurboff, Steve Cosentino

Motorola Inc., 1000 Technology Way, Libertyville, IL 60048

Abstract -- **In this paper, we review recently published SiGe BiCMOS technologies for RFIC design. Performance and integration trends in SiGe HBT's are discussed. Performance of passive devices, such as an inductor, plays a key role in RF design. We review approaches to realize high Q inductor on a Si substrate. Finally, interaction of HBT performance with design is illustrated through LNA design**

I. INTRODUCTION

SiGe based BiCMOS technology has become a key technology for RFIC design as evident by product and technology announcements from several companies. The goal of this paper is to review advanced SiGe process technology from the perspective of designers and to provide an overview of the key aspects of the technology, which are important in the RFIC design process. The details of the fabrication technology can be found in process technology intensive papers [1-16].

II. MODULAR SiGe PROCESS TECHNOLOGY

Digital CMOS technology is the driver for core semiconductor process modules, such as development of advanced lithography or ultrathin gate oxide, and is generally a generation or two ahead of the BiCMOS technology. Hence, a cost effective way to deliver BiCMOS technology is to provide a modular integration of SiGe HBT into mainstream CMOS technology. Figure 1 shows an example of modular integration approaches adopted by several companies including Motorola [1-3].

There are RF performance drawbacks if modular integration is done on low resistivity substrates which are used in CMOS processes for latchup immunity. The low substrate resistivity negatively impacts the inductor Q and increases RF loss. The RF performance is improved by migrating the baseline BiCMOS process to a higher resistivity wafer. In addition to cost reductions, modular integration of HBT's enables reuse of CMOS design blocks. Several recent publications [1-3] showed that modular integration of HBT's doesn't have any significant impact on the parent MOS characteristics further reinforcing the concept of digital design reuse.

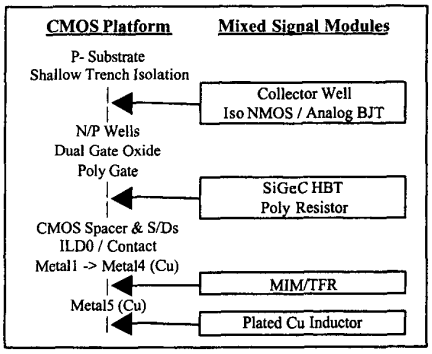

Fig 1. Modular integration approach adopted by Motorola [1].

III. SiGe HBT PERFORMANCE TRENDS

Aggressive lateral and vertical scaling have led to tremendous improvement in raw performance of SiGe HBT's (Fig 2). Figure 3 shows a plot of unity gain cut-off frequency (f_T) versus BVceo. For 2.5-3.0 V designs, an f_T of 50 GHz is typical and for 1.8-2.0 V designs f_T's of 100 GHz are beginning to appear.

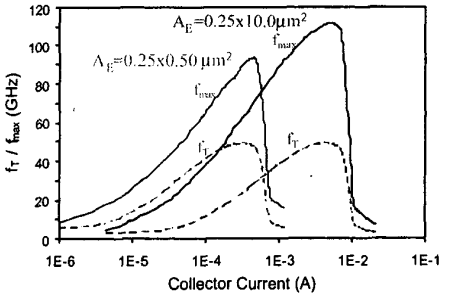

Fig 2. f_T and f_{MAX} versus collector current SiGe:C HBT devices (Vce=2V) integrated on Motorola's 0.18 μm CMOS technology. [1]

0-7803-7239-5/02/$10.00 © 2002 IEEE

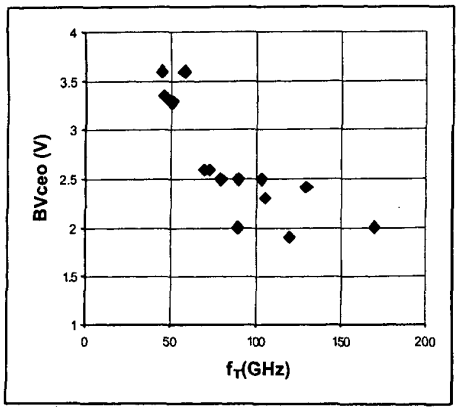

Fig 3. Shows performance of SiGe HBT's reported in BCTM and IEDM conferences between 2000-2001[1-16]

Peak cut-off frequency is a useful benchmark when SiGe HBT's are used to design very high-speed digital circuits. For low noise applications, such as LNA's in a wireless transceiver, low current performance of HBT's is critical. The noise minima in an HBT occur at a low collector current density (around 0.1 mA/μm^2), because of competing contribution of thermal noise and shot noise. A review of f_T versus collector current for the HBT's shown in Fig 3 reveal that the cut-off frequency at 0.1 mA/μm^2 collector current density is around 20 GHz for most of the technologies even though peak cut-off frequencies vary significantly between them.

A more useful indicator of performance for low noise application is f_{MAX}, which includes the effect of base resistance. Aggressive lateral scaling and advanced processing techniques, such as carbon doped base layer [1-2], have led to significant reduction in base resistance. Figure 4 shows a plot of f_T vs. f_{MAX} for the transistors of Fig 3. For low noise applications, such as a 2 GHz LNA for wireless handsets, an HBT with 50 GHz f_T and highest possible f_{MAX} would be desirable.

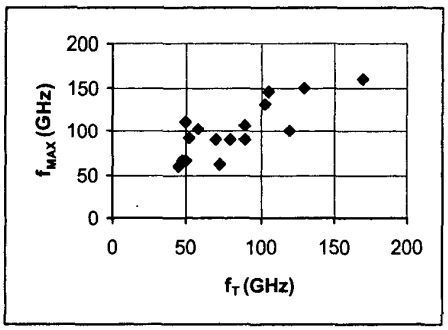

Fig 4. f_{MAX} of HBT's in Fig 3 are plotted against f_T

IV. PASSIVES

Commercially available SiGe technologies come with a full array of passive devices. Table 1 lists a representative sample of passive devices in 0.18um BiCMOS technology at Motorola [1].

TABLE I
KEY PASSIVE ELEMENT PARAMETERS

Resistor		**Polysilicon**	**TFR**
Sheet Resistance	ohm/sq	1500	50
Linearity	ppm/V	75	10
TCR	ppm/C	-1400	-100
Mismatch	1 sigma	<1 %	<0.5%
1/f corner	Hz	--	<50

Capacitor		**Gate**	**MIM**
Specific Capacitance	fF/μm^2	8	1.6
Linearity	ppm/V	--	-15
TCR	ppm/C	--	8
Mismatch	1 sigma	--	<0.05%

Inductor	**Plated Copper**
Q @2 GHz	18 for L=3 nH

High Q inductors are key to most RFIC designs. For example, power loss and phase noise in a VCO decrease quadratically as Q increases. On the other hand, Si substrate is more lossy as compared to semi-insulating GaAs. Hence, designing high Q integrated passives in Si based technologies is challenging.

Approaches to generate high Q inductors are: a) reduce resistance of the coil, b) make the dielectric layer underneath the coil as thick as possible, c) reduce substrate loss, d) if possible, connect the inductor differentially to reduce capacitance to ground. The first two items are in the technology offered whereas the last two items are under the control of designers. Most of the SiGe BiCMOS technologies [1-18] offer a thick Al top metal layer of thickness 3-4 um for inductor design. In Motorola's 0.18 µm BiCMOS technology, a 10 µm thick electroplated copper with sheet resistance of 2mOhm/sqr is used for inductor design. Figure 5 shows SEM view of an electroplated copper inductor and its measured characteristics.

Moving inductor coils to a higher level of metallization improves Q but it requires an additional metal layer and is not cost effective. Using a higher resistivity substrate can reduce substrate loss but excessively resistive substrate makes CMOS devices more

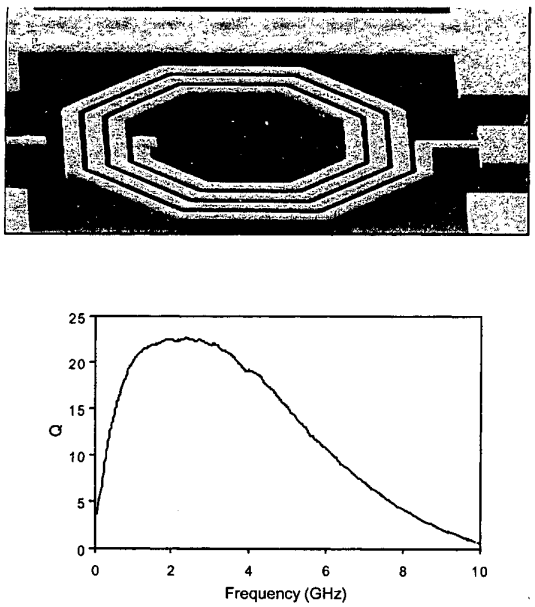

Fig 5. SEM cross-section of an electroplated inductor built on top of the last metal layer. A Q >20 can be achieved with a 3 nH inductor [1].

prone to latch-up. Alternatively, deep trenches underneath the inductor can be used to reduce substrate losses. Another interesting technique to improve inductor Q is to connect the inductor differentially [19]. An improvement of Q factor by 30% was observed by exciting the coil differentially (Fig. 6).

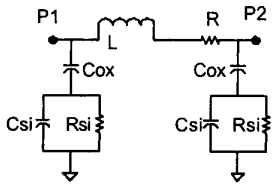

Fig 6. Single port excitation shorts capacitance to ground on one of the ports whereas differential excitation puts the impedance to ground in series.

MIM capacitors offered in all SiGe BiCMOS technologies [1-16] have a high Q and excellent linearity, which makes it suitable for RFIC applications. Capacitance density in SiGe technologies range between 1 to 2 fF/μm^2 and some MIM caps are as high as 5 fF/μm^2 [20]. Q factor in excess of 50 can be achieved at 2 GHz. Higher MIM cap density can also be realized by stacking MIM capacitors on multiple metal layers.

V. Design Issues

In order to derive maximum benefit out of a given technology, design of RFIC blocks has to be tuned to a particular technology. We will illustrate the interaction of technology with design through the design steps of a 2.1GHz common emitter LNA where emitter length of the LNA is varied to obtain noise and power match [21-23].

The first step is to analyze a unit device to determine the bias condition for minimum noise. Figure 7a shows that for a 0.25x10 μm HBT, the minimum NF attainable is approximately 0.6 dB at a current of 0.2 mA. However, to realize 0.6dB NF, we need to drive the amplifier with 800 Ohm source impedance as shown in Fig 7b. For a 50 Ohm source impedance, we need to connect 16 emitters in parallel and bias it at 3.2 mA to achieve noise matching. Figure 8 shows that the optimum bias is about 4 mA.

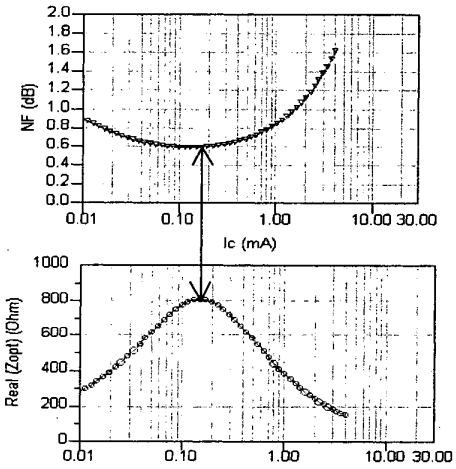

Fig 7 a) Simulated Minimum Noise Figure in a 10x0.25 μm HBT; b) Optimum source resistance for noise matching.

Front-end RFIC's in wireless transceivers are typically preceded by SAW filters. To reduce power consumption and attain minimum noise figures in LNA's, one could use a high impedance SAW filters. For example, to noise-match the above transistor to a 100 Ohm SAW, one would use approximately 8 emitters and bias it at 2 mA. A series inductor in the emitter and another at the base of the transistor enable power matching once the noise matching is done [23]. The measured noise figure on ICs will be somewhat higher because of the losses in the inductors and bond wires, and due to the impact of interconnect parasitics. Since, the transistor will be operating at low current levels to minimize noise, particular attention has to be paid to the layout of the circuit to minimize

interconnect crossover capacitances, some of which will act like miller capacitance and reduce gain. Effective substrate isolation of LNA's, such as use of p+ guard ring or isolated pwell, is also critical in p- substrates to reduce noise coupled from other blocks in the IC [24]. In wide band receivers, higher IP3 spec might require increase in current but by optimizing near the noise minima, impact of increased bias current on NF is minimized.

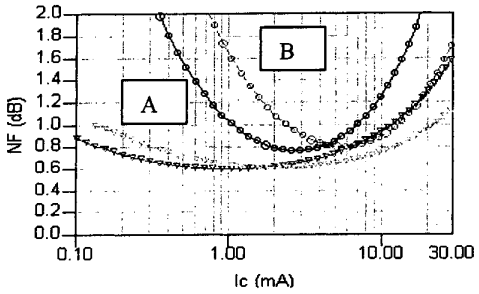

Fig 8 Triangles are NFmin, circles are NF. Two NF figure plots are for 100 ohm (A) and 50 ohm (B) source impedance.

VI. SUMMARY

We surveyed key components of SiGe BiCMOS technology. Modular integration of HBT on a CMOS platform was found to be the common trend to reduce cost and aid reuse of models and designs. Design of a high Q integrated inductor is a challenge on Si substrate. Design based as well as technology based techniques have to be adopted to improve Q factor of an integrated inductor. For low noise RFIC design, often quoted peak performance metrics, such as peak, f_T may not be a good benchmark. We should focus more on low current performance where noise is at its minimum.

ACKNOWLEDGEMENTS

Many thanks to Motorola SPS Digital DNA Laboratories and WITC/WBSG for their support

REFERENCES

[1] J. Kirchgessner et al., "A 0.18µm SiGe:C RFBiCMOS Technology for Wireless and Gigabit Optical Communication Application", *BCTM, pp.151, 2001*

[2] F. K. Chai et al., " A Cost-Effective 0.25µm Leff BiCMOS Technology Featuring Graded-Channel CMOS (GCMOS) and a Quasi-Self-Aligned (QSA) NPN for RF Wireless Applications" *BCTM,* pp. 110, 2000

[3] D. Harame et al., "Current Status and Future Trend of SiGe BiCMOS Technology", *Tran. E-D,* pp. 2575, Nov 2001

[4] L. C. M. van den Oever, et al., "Design of 200GHz SiGe HBT's", *BCTM,* pp. 78, 2001

[5] F. S. Johnson et al., "A Highly Manufacturable 0.25µm RF Technology Utilizing a Unique SiGe Integration", *BCTM,* pp. 56, 2001

[6] H. Baudry et al., "High performance 0.25µm SiGe and SiGe:C HBTs using non selective epitaxy", *BCTM,* pp. 52, 2001

[7] P. Deixler et al. "Exploration for High Performance SiGe-Heterojunction Bipolar Transistor Integration", *BCTM,* pp. 52, 2001

[8] A. Joseph et al., "A 0.18µm BiCMOS Technology Featuring 120/100 GHz (f_T/f_{MAX}) HBT and ASIC-Compatible CMOS Using Copper Interconnect", *BCTM,* pp. 143, 2001

[9] K. Schuegraf et al., "0.18µm SiGe BiCMOS Technology for Wireless and 40Gb/s Communication Products", *BCTM,* pp.147, 2001

[10] A. Gruehle "Prospects for 200GHz on Silicon SiGe Heterojunction Bipolar Transistors", *BCTM,* pp. 19, 2001

[11] J. Boeck et al., "High-Speed SiGe:C Bipolar Technology", *IEDM,* pp. 344, 2001

[12] M. Racanelli et al., "Ultra High Speed SiGe NPN for Advanced BiCMOS Technology", *IEDM,* pp336, 2001

[13] D. Heinemann et al., "Cost-Effective High-Performance High-Voltage SiGe:C HBTs with 100GHz f_T and BV_{CEO} x f_T Products Exceeding 220VGHz", *IEDM,* pp. 348, 2001

[14] D, Knoll et al., "HBT before CMOS, a New Modular SiGe BiCMOS Integration Scheme", *IEDM,* pp. 499-503, 2001

[15] S. Decoutere et al., "A 0.35µm SiGe BiCMOS Process Featuring a 80 GHz Fmax HBT and Integrated High-Q RF Passive Components, *BCTM,* pp. 106, 2000

[16] R. Tang et al., "A Low-Cost Modular SiGe BiCMOS Technology and Analog Passives for High-Performance RF and Wide-Band Applications", *BCTM,* pp. 102, 2000

[17] R. Groves et al., "High Q Inductors in SiGe BiCMOS Process Utilizing a Thick Metal Process Add-on Module", *BCTM,* pp. 149, 1999

[18] C. P. Yue et al., "On-Chip Spiral Inductors with Reduced Ground Shields for Si-Based RF IC's", *JSSC, Vol. 33, pp. 743, 1998*

[19] M. Danesh et al., " A Q Factor Enhancement Technique for MMIC Inductors", *RFIC Symp.* pp.217, 1998

[20] D. Szmyd et al., "QUBIC4: A Silicon RF-BiCMOS Technology for Wireless Communication ICs, *BCTM,* pp. 60, 2001

[21] D. Greenberg et al., "Noise Performance and Considerations for Integrated RF/Analog/Mixed Signal Design in a High Performance SiGe BiCMOS Technology", *IEDM,* pp. 336, 2001

[22] S. Voingescu et al., "A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low Noise Amplifier Design", JSSC, Vol 32, pp. 1430, 1997

[23] O. Shana's et al., "Frequency Scalable SiGe Bipolar RF Front-End Design", JSSC, Vol 36, pp. 888, 2001

[24] K. To et al., "Comprehensive Study of Substrate Noise Isolation for Mixed-Signal Circuits" *IEDM, pp. 519, 2001*